Amendments to Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims:

Claim 1. (Original) A data communications interface for a node of data processing network, the interface comprising:

- a data transmission path;
- a transmission control path:

transmission segmentation logic for receiving a data frame, comprising a transmission header and a transmission payload, from the node and supplying the transmission payload to the data transmission path and the transmission header to the transmission control path;

a transmission processor in the transmission control path for controlling communication of data from the transmission payload to the network via the data transmission path in dependence on the transmission header;

- a data reception path;
- a reception control path;

reception segmentation logic for receiving a data packet, comprising a reception header and a reception payload, from the network and supplying the reception payload to the data reception path and the reception header to the reception control path; and,

a reception processor in the reception control path for controlling communication of data from the reception payload to the node via the data reception path in dependence on the reception header.

Claim 2. (Original) An interface as claimed in claim 1, comprising a shared memory and a local bus providing access to the shared memory by the transmission and reception processors.

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An interface as claimed in claim 2 wherein the Claim 3. (Currently Amended) shared memory comprises a store for control information to be used by the transmission and reception processors in controlling said flows of data.

Claim 4. (Previously Presented) An interface as claimed in claim 2 comprising a communication path for communicating information between the transmission and reception processors via the shared memory.

Claim 5. (Currently Amended) An interface as claimed in claim 1, comprising bus interface logic for connecting the a local bus, the transmission data channel, and the reception data channel to a bus architecture of the node.

Claim 6. (Previously Presented) An application specific integrated circuit, comprising a data communication interface as claimed in claim 1.

Claim 7. (Previously Presented) A network interface card for insertion into a computer system, the network interface card comprising a printed circuit board and a data communications interface as claimed in claim 1 mounted on the printed circuit board.

Claim 8. (Previously Presented) A computer system comprising: a central processing unit; a memory; a data communications interface as claimed in claim 1; and, a bus architecture interconnecting the central processing unit, the memory, and the data communications interface.

A data processing network as recited in claim Claim 9. (Currently Amended) 8, comprising a plurality of computer systems as claimed in claim 8 and a network architecture interconnected to the computer systems.

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receiving, via transmission segmentation logic, a data frame, comprising a transmission header and a transmission payload, from the node;

supplying, via the transmission segmentation logic, the transmission payload to a data transmission path and the transmission header to a transmission control path;

controlling, via a transmission processor in the transmission control path, communication of data from the transmission payload to the network via the data transmission path in dependence on the transmission header;

receiving, via reception segmentation logic, a data packet, comprising a reception header and a reception payload, from the network;

supplying, via the reception segmentation logic, the reception payload to a data reception path and the reception header to a reception control path; and,

controlling, via a reception processor in the reception control path, communication of data from the reception payload to the via the data reception path in dependence on the reception header.

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